CoE 1541 Project 2 Data Analysis

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As seen in the excel file with all of the sample trace data there is a very strong correlation between cache size and L1 miss rate. As the cache size grew there was a lower and lower L1 miss rate for every different block size. This is because as the cache size grows you can keep more and more data within it and when the time comes to access data you are more likely to have that data still in the cache. The L2 cache tended towards an opposite correlation than that of the L1 cache. As cache size grew the L2 miss rate tended to rise slightly. This is mostly due to the fact that as we get less L1 misses and that the times we do miss are more likely to be data that haven’t been used yet, or haven’t been used for a very long time. Due to the lower L1 miss rate as cache size increases we also tend towards having less cycles per trace. This is because as we hit more in L1, we access L2 and memory less.

A change in the block size didn’t have as strong of a correlation as that of the cache size. For the smaller cache size samples, the bigger the block size wasn’t ideal. Rather, you would want to have a 16 or 64 B block size to improve L1 miss rate. For the larger cache size samples, larger block sizes tend to result in better L1 miss rates. For all cache size traces, the L2 miss rate worked in inverse with the L1 miss rate, as explained in the above paragraph. The cycle amount for each trace follows the same trend as the L1 miss rate.